## AMENDMENT

**In The Claims:**

Please amend the claims as follows:

Claim 1. (currently amended) A method of testing a chip that comprises an intellectual product circuit module, the method comprising:

providing a test pattern ~~through a plurality of input lines~~;

sequentially enabling a common storage device to store ~~storing configuring a plurality of registers with~~ the test pattern based on ~~in~~ a plurality of different states ~~according to the test pattern~~; and

after the test pattern is stored in the common storage device ~~all of the registers are configured with the test pattern~~, selecting one of the intellectual product circuit modules according to the test pattern for testing and providing the a test activating signal with a synchronous clock signal to the selected intellectual product circuit modules in a next state, so that the selected intellectual product circuit modules is operated and tested according to the test pattern from the ~~registers~~ common storage device.

Claim 2. (currently amended) A circuit for testing a chip that comprises an intellectual product circuit module, the circuit for testing the chip further comprising:

~~a plurality of registers~~ a common storage device, coupled to the intellectual product circuit module ~~to output signals stored in the registers to the intellectual product circuit module~~; and

an input signal selector ~~multiplexing finite state machine controller~~, coupled to the intellectual product circuit module and the common storage device ~~registers~~, wherein

the ~~multiplexing finite state machine controller~~ input signal selector receives a test pattern and sequentially enabling the common storage device to store the test pattern based on ~~configures the registers with the test pattern in~~ a plurality of different states, after ~~all of the registers are configured with~~ all of the test pattern is stored in the common storage device, in a next state the ~~multiplexing finite state machine controller~~ input signal selector further provides a test activating signal with a synchronous clock signal to the intellectual product circuit module so that the intellectual product circuit module is operated and tested according to outputs of the common storage device ~~registers~~.

Claim 3. (currently amended) The circuit according to claim 2, wherein the intellectual product circuit module further comprises a plurality of ports coupled to the common storage device ~~registers~~.

**Claim 4. (cancelled)**

Claim 5. (currently amended) The circuit according to claim 2, wherein ~~each of~~ the common storage device ~~registers~~ further comprises an enable input terminal coupled to the ~~multiplexing finite state machine controller~~ input signal selector capable of controlling the common storage device ~~registers~~ and asserting an enable signal to enable the common storage device ~~registers~~ to buffer the test pattern.

Claim 6. (currently amended) A circuit for testing a chip that comprises a plurality of intellectual product circuit modules, the circuit comprising:

an output selector ~~multiplexer controller~~, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules;

~~a plurality of registers~~ a common storage device, coupled to the intellectual product circuit modules to output signals stored in the common storage device ~~registers~~ to the intellectual product circuit modules; and

a ~~multiplexing finite state machine controller~~ input signal selector, coupled to the intellectual product circuit modules, the output selector ~~multiplexer controller~~ and the ~~registers~~ common storage device, the ~~multiplexing finite state machine controller~~ input signal selector for receiving a test pattern ~~from a plurality of input lines~~ and ~~to~~ sequentially enabling the common storage device to store the test pattern base on ~~configuring the registers with the test pattern in~~ a plurality of different states of the ~~multiplexing finite state machine controller~~ input signal selector, and after all of the test pattern is stored in the common storage device ~~registers are configured with the test pattern~~, selecting one of the intellectual product circuit modules according to the test pattern for testing and providing a test activating signal with a synchronous clock signal to the selected one of the intellectual product circuit modules in a next state, so that the selected intellectual product circuit module is operated and tested according to the output of the common storage device ~~registers~~, and the ~~multiplexing finite state machine controller~~ input signal selector further controlling the output selector ~~multiplexer controller~~ to selectively output the test results.

Claim 7. (currently amended) The circuit according to claim 6, wherein each of the intellectual product circuit modules comprises a plurality of ports coupled to the ~~registers~~ common storage device.

Claim 8. (currently amended) The circuit according to claim 6, wherein the output selector ~~multiplexer controller~~ further comprises a select input terminal coupled to the ~~multiplexing finite state machine controller~~ input signal selector, so that the ~~multiplexing finite state machine controller~~ input signal selector controls the output selector ~~multiplexer controller~~ to selectively output the test result.

**Claim 9. (cancelled)**

Claim 10. (currently amended) The circuit according to claim 6, wherein ~~each of~~ the common storage device ~~registers~~ further comprises an enable input terminal coupled to the ~~multiplexing finite state machine controller~~ input signal selector, which respectively controls and enables the common storage device ~~registers~~ to buffer the test pattern.

Claim 11. (original) The circuit according to claim 6, wherein the chip is a system on chip.